VPX55HS-3, 3U VPX DC/DC Converter

Made in the USA
Certified Small Business

750-Watt Ruggedized Converter
Developed in alignment with the SOSA™ Technical Standard
Plug-in Module, Conduction-Cooled, Six Outputs

Description

NAI's VPX55HS-3 is a 750 Watt DC/DC Converter that plugs directly into a standard 3U VPX chassis with a VITA 62, 1.0" power supply slot. This off-the-shelf solution for VITA 46.0 and VITA 65 systems is compatible with VPX specifications; supports all VITA standard I/O, signals, and features; and conforms to the VITA 62 mechanical and electrical requirements for modular power supplies. Contains Integrated IPMC, with Dual Bus IPMB-A, IPMB-B,

The VPX55HS-3 supply is conduction-cooled through the card edge/wedgelock. It accepts +28 VDC input voltage and provides up to six outputs per VITA 62 at up to 750 Watts with an option for the SOSA™ (+12 Volt Only) configuration. It supports a variety of standard features including continuous Background Built-In-Test (BIT), I^2C communication, remote error sensing, current share and protection against transients, overvoltage, overcurrent, over-temperature and short-circuits. With its intelligent design, the VPX55HS-3 also has the flexibility to address special needs.

Features

- Ideal for rugged 3U VPX power applications
- Standard VPX-compatible connectors and I/O per VITA 62
- System Management Bus per VITA 46.11
- IPMC Dual Bus IPMB-A & IPMB-B
- Off-the-shelf solution for VITA 46.0 and VITA 65 systems
- Supports all VITA standard I/O, signals, and features
- Accepts +28 VDC input
- Provides six outputs and I/O at up to 750 Watts
- **SOSA™** Aligned output configuration
- Continuous Background Built-in-Test (BIT)
- User Programmable
- Current share
- Input transient protection per MIL-STD-704F
- EMI per MIL-STD-461F
- Environmentals per MIL-STD-810H and VITA 47.1 ECC4SL1
- Operates at full load through the entire -40°C to +85°C temperature range

116 Wilbur Place, Bohemia, NY 11716 Tel: 631.567.1100 www.naii.com

Electrical Specifications

DC Input Characteristics	
Input	+28 VDC (+18 VDC to +40 VDC range)
EMI/RFI	Designed to meet the requirements of MIL-STD-461F; CE102 compliant (additional system filtering required)
Input Transient Protection	Ride-through Normal transients Per MIL-STD-704F. No damage when subjected to abnormal transients and power interruption
Output Power	750W max at 85°C (see Output Power Table)
Output Voltage	Standard VPX outputs, Heavy +12V or +12V only per SOSA™ (see Output Power Table)
Efficiency	91% typical for SOSA +12V only; 89% typical for other output configurations. Measured @ full load
Switching Frequency	Main Converter 150kHz, Secondary Converters 300kHz
Line Regulation	Within 0.5% or 20 mV (whichever is greater) for low to high line changes at constant load. For current share units: 1.5% for VS1, VS2, VS3; 2% for +3.3 VDC_Aux, +12 VDC_Aux, -12 VDC_Aux
Load Regulation	0.5% or 20 mV (whichever is greater) for 0 to 100% of rated load at nominal input line with remote sense. 1% for -12 VDC_Aux, +12 VDC_Aux, +3.3 VDC_Aux; For current share units: 1.5% for VS1, VS2, VS3, +3.3 VDC_Aux; 2% for +12 VDC_Aux, -12 VDC_Aux
PARD (Noise and Ripple)	1% or 50 mV p-p max per VITA 62; measurements are made with a 20 MHz bandwidth instrument connected on load wires < 5 inches from power supply and terminated with 1uF capacitors across load lines
Load Transient Recovery	Output voltage returns to regulation limits within 0.5 msec, half to full load
Load Transient Under/Overshoot	5% of nominal output voltage set point (1.4 V max); 2.5% for VS3
Short Circuit Protection	Protected for continuous short circuit with automatic recovery
Current Limiting	All outputs to 130%
Over Voltage Protection	Automatic electronic shutdown if outputs exceed 125% ±10%
Remote Error Sensing	Sensing pins compensate for up to 0.5 V drop on VS1 to VS3 outputs
Isolation Voltage	500 VDC input to output and input to case; 100 VDC output to case
Insulation Resistance	50 Mega Ohm at 500 VDC

All specifications are subject to change without notice.

116 Wilbur Place, Bohemia, NY 11716 Tel: 631.567.1100 www.naii.com

Additional Specifications

Physical/Environmental	
Temperature Range	Operating: -40°C to +85°C at 100% load. Temperature measured at card edge, conduction via card edge. Storage: -55°C to +105°C per VITA 47 CC4.
Temperature Coefficient	0.01% per °C
Shock	40 G's each axis per MIL-STD-810H, Method 516, Procedure 1. VITA 47 OS2
Acceleration	6 G's per MIL-STD-810H, Method 513, Procedure II
Vibration	Per MIL-STD-810H, Method 514, Procedure 1; 12 GRMS, VITA 47, Class V3
Humidity	95% at 71°C per MIL-STD-810H, Method 507 (non-condensing)
Altitude	1,500 feet below sea level to +60,000 feet above sea level per VITA 47
Salt & Fog	Per MIL-STD-810H, Method 509, VITA 47 Class SL1.
Sand/Dust	Per MIL-STD-810H, Method 510
Fungus	Per MIL-STD-810H, Method 508
ESD	15 kV EN61000-4-2 per VITA 47
Enclosure	Aluminum housing to aluminum baseplate
Dimensions	See Mechanical Layout
Finish	Chemical film IAW MIL-DTL-5541, Type II, Class 3
Interface	50 Micro-Inch Gold on contacts; plated tails for tin whisker mitigation; See connector specifications table
Weight	1.6 lbs. Typical

All specifications are subject to change without notice.

116 Wilbur Place, Bohemia, NY 11716 Tel: 631.567.1100 www.naii.com

Signal Types

Signal	Description
ENABLE*	Turns off all of the output voltages, including 3.3 V_AUX, when signal is High. ENABLE* is pulled Low by using a mechanical switch which connects it to SIGNAL_RETURN. A Logic output can also be used to drive the ENABLE*. Opening the switch would turn off all the outputs; closing the switch or applying the Logic output would enable the outputs to come on depending on the state of INHIBIT*. An input of <0.8 VDC is regarded as a Low and an input of >2.0 VDC is regarded as a High. A no-connect is also regarded as a High. Along with INHIBIT*, this signal determines the output power status of the VPX55HS-3 (see Power Status Table below).
INHIBIT*	Turns off all the output voltages. In most implementations, the signal is expected to leave 3.3 V_AUX on. Pulling INHIBIT* Low turns off VS1, VS2, VS3, and ±12 VDC_Aux outputs. An input of <0.8 VDC is regarded as a Low and an input of >2.0 VDC is regarded as a High. A no-connect is also regarded as a High. Along with ENABLE*, this signal determines the output power status of the VPX55HS-3 (see Power Status Table below).
SYSRESET*	An active low open-collector line driven by the Power Monitor module. Signal ensures a clean, stabilized startup based on monitoring the output voltage levels in accordance with VITA 46.0, paragraph 4.8.11. Timing can be factory customized.
FAIL*	Indicates failure when any of the outputs are not within specification. Signal complies with VITA 65 for active Low. FAIL* signal is Open Drain. It is expected that there will be a pull-up resistor on the backplane.
VBAT	Provides a low-power +3.3 VDC @ 1A output to other plug-in modules. Intent is to supply power to low current devices, such as Real Time Clocks, when other outputs are off. While connected internally to the +3.3 VDC_Aux output, the signal provides a separate line dedicated to low power needs and has its own overcurrent protection. The signal is controlled thru power status, along with the +3.3 VDC_Aux output (see Power Status Table below).
Geographical Addressing	As defined in VITA 46
Current Share	Allows multiple supplies to share system load for VS1-VS3 outputs. Optional, refer to ordering information.
Protocol	Per VITA 46.11 System Management Bus.
Status LED	See LED Status table below

LED Status

LED State	Meaning
Off	Input Low
Green (Steady)	Vout OK; All outputs are good
Red (Steady)	Fail; Follows same logic as FAIL* signal
Blinking Green	Unit disabled
Blinking Red	Over Voltage or Over Temperature (all outputs are off)

Power Status

Control Input States		Power Output States	
ENABLE*	INHIBIT*	+3.3V_AUX	VS1, VS2, VS3, +12V_AUX & -12V_AUX
High	High	Off	Off
High	Low	Off	Off
Low	High	On	On
Low	Low	On	Off

116 Wilbur Place, Bohemia, NY 11716 Tel: 631.567.1100 www.naii.com

I²C Communication

Mode I - VITA 46.11 Tier 2 dual bus

Provides all mandatory Sensor Data Record (SDR) and all required FRU data as well as real-time analog data

1. **Hardware Interface.**
   Electrical interface is based on I2C parameters at 100 kHz. The backplane or I2C master controller should provide pull up resistors on SDA and SCL lines to a 3.3V rail.

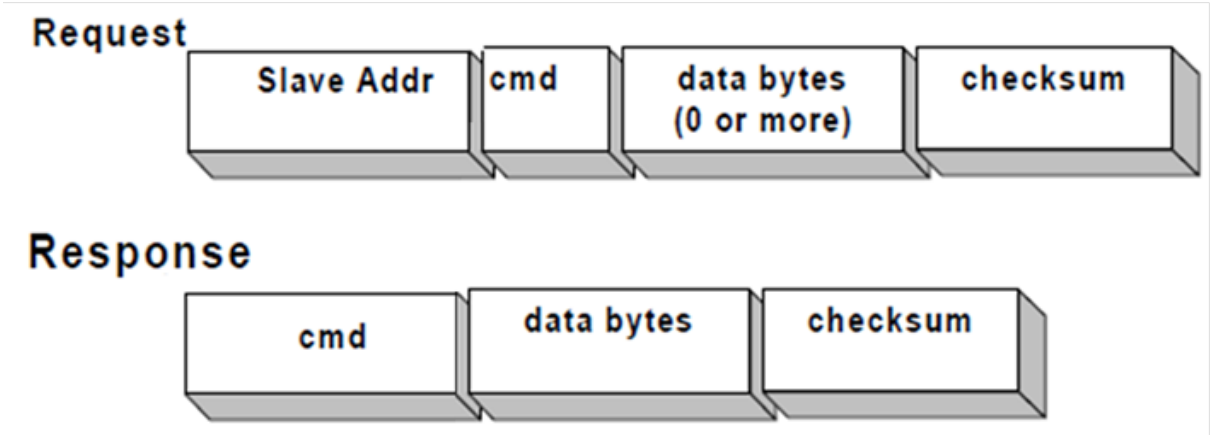
2. **Address.**
   The I2C Address is 7 bits. Default base address is 0x20. *GA0, and *GA1 provides 2 LSB's for the address.

   The *GA pins have pull-up resistors internal to the power supply to 3.3V. When left open, the address will be 0x20, with both grounded the address will be 0x23, see table below.

Pin		I2C Address
*GA1 Pin B5	*GA0 Pin A5	
High	High	0x20
High	Gnd	0x21
Gnd	High	0x22
Gnd	Gnd	0x23

Mode II - Legacy Slave Mode Commands (*Available via ejector panel communication port*)

1. **Supports Legacy Slave Mode Commands**
   Data Read - Get Sensor Reading results



116 Wilbur Place, Bohemia, NY 11716 Tel: 631.567.1100 www.naii.com

	Byte	Data Field	Data
Request Data	1	cmd	See table
	2 to n-1	Data If Required by cmd or Zero ChkSum* if no Data required.	
	n	Zero ChkSum* if Data was required by cmd	
Response Data	1	Completion Code – Echo cmd Number	
	2 to n-1	Per cmd Response	
	n	Zero ChkSum	

Note : Slave address should not be included in Zero Checksum calculation.

2. Commands

Sensor #	Name	Description
21H	Composite Sensor	64 bytes of scanned sensor data. Data is continually scanned and available for report. Data consists of 2 bytes of data for each of the 11 sensors and FRU data.
55H	Status Write Command	Writes Status byte on Composite Sensor.
44H	Firmware release date	22 byte response. Month/Day/Year Hr/Min/Sec in ASCII form.
45H	Hardware Address	3 byte response. Reports address set by GA0*-GA1*

3. Composite Sensor Read Command – 21H

Response BYTE #	Data Type	Meaning
0	Completion Code – 21h	Echo of the command
1	Status Register 0, MS Bit First	Refer to table below
2-3	Signed Integer, MSB First	Temperature as follows °C = (Reading * 100 / 16384)
4-5	U Integer, MSB First	Voltage on VS1, 12V = 16384
6-7	U Integer, MSB First	Voltage on VS2, 3.3 = 16384
8-9	U Integer, MSB First	Voltage on VS3, 5V = 16384
10-11	U Integer, MSB First	Voltage on 3.3Aux, 3.3V = 16384
12-13	U Integer, MSB First	Voltage on +12V Aux, 12V = 16384
14-15	U Integer, MSB First	Absolute Voltage on -12V Aux, 12V = 16384
16-17	U Integer, MSB First	Full Load current on VS1 = 16384
18-19	U Integer, MSB First	Full Load current on VS2 = 16384
20-21	U Integer, MSB First	Full Load current on VS3 = 16384
22-23	U Integer, MSB First	Full Load current on 3.3Aux = 16384
24-25	U Integer, MSB First	Full Load current on +12VAux = 16384
26-27	U Integer, MSB First	Absolute Full Load current on -12Vaux = 16384
28-29	U Integer, MSB First	Internal Reference, 2.5V = 16384
30-31	U Integer, MSB First	Input Voltage 28V = 16384
32-51	Character String	Part Number
52-53	U Integer, MSB First	S/N Hi
54-55	U Integer, MSB First	S/N Low
56-57	U Integer, MSB First	Date Code (Year/Week)
58-59	Character String	Hardware Rev
60-61	Character String	Firmware Rev
62	Reserved	Reserved
63	Zero Checksum	Value required to make the sum of bytes 0 to 62 add to a multiple of 256 (decimal).

116 Wilbur Place, Bohemia, NY 11716 Tel: 631.567.1100 www.naii.com

Status Reg 0		R/Set	R/Set	R/W	R/W	R/W	R	R
Bit	7	6	5	4	3	2	1	0
	x	FAIL	OTWarning	SWPriority	*SW Inh	*SW En	*HW Inh	*HW En

Bits 5 AND 6 (OTWarning - FAIL) are Read and write. They are clear at startup. User can set them with a Status Write command. Hardware will clear them if there is a fault.
Bit 4 (SWPriority) is Read and write. It is clear at Startup. When clear the unit will be controlled by the hardware enable and inhibit signals. When set, the unit will be controlled by the SW inhibit and enable signals.

Bits 3 and 2 (SWInh SWEn) are read and write. Their logic works the same as the logic for the hardware Enable and Inhibit.

*SWEnable	*SWInhibit	OUTPUTS
0	0	INHIBIT (3.3V Aux is On, all other outputs are off)
0	1	ON
1	0	OFF
1	1	OFF

Bits 1 and 0 (HWIn - HWEn) are read only. They show the state of *Enable and *Inhibit pins while SWPriority is low.

4. Status Write Command - 55H

BYTE #	Data Type	Meaning
0	U Character – 55H	Command
1	U Character	Data
2	Zero Checksum	Value required to make the sum of bytes 0 and 1 add to a multiple of 256 (decimal).

The command to write to Status byte is 55h, followed by 8-bit data then zero checksum.

Example: To send a command to clear the faults and turn on all the outputs, the following sequence must be sent.
55h 78h 33h;
55h is the command needed to write to status byte zero.
78h data for byte zero,
Bit 7 set: don't care bit.
Bit 6 set: FAIL signal is high, software will clear it if unit fails
Bit 5 set: OTWarning signal is high, software will clear it if unit is close to 75 degrees.
Bit 4 set: Software has priority to enable/disable unit.
Bit 3 set: SWInhibit is high
Bit 2 low: SWEnable is low.
33h Value to achieve a sum of zero.

5. Firmware release date – 44H

Response BYTE #	Data Type	Meaning
0	Completion Code – 44H	Echo of the command
1-20	Character String	Date
21	Zero Checksum	Value required to make the sum of bytes 0 to 20 add to a multiple of 256 (decimal).

6. Hardware Address – 45H

Response BYTE #	Data Type	Meaning
0	Completion Code – 45H	Echo of the command
1	U Character	I2C Hardware Address
2	Zero Checksum	Value required to make the sum of bytes 0 and 1 add to a multiple of 256 (decimal).

116 Wilbur Place, Bohemia, NY 11716 Tel: 631.567.1100 www.naii.com

Output Configurations

750 Watt Power (refer to Notes Below)									
	Standard Output Configuration			+12V Heavy Configuration			+12V Only Configuration per SOSA™		
Pin Number	Designation (Power Form)	Volts	Amps	Designation (Power Form)	Volts	Amps	Designation (Power Form)	Volts	Amps
P6	VS1 (PO1)	+12Vdc	40	VS1 (PO1)	+12Vdc	60*	VS1 (PO1)	+12Vdc	60*
LP2	VS2 (PO2)	+3.3Vdc	20	VS2 (PO2)	+3.3Vdc	20	+3.3V_Aux	+3.3Vdc	20
P3	VS3 (PO3)	+5Vdc	40	VS1 (PO1)	+12Vdc	60*	VS1 (PO1)	+12Vdc	60*
B3	+12V_Aux	+12Vdc	1	+12V_Aux	+12Vdc	1			
C6	-12V_Aux	-12Vdc	1	-12V_Aux	-12Vdc	1			
A4,B4,C4,D4	+3.3V_Aux	+3.3Vdc	4	+3.3V_Aux	+3.3Vdc	4			

***Total of 60A capability from PO1 combined**

**** Total Power limited to 750W at 85°C**

Connector Specifications

Unit	Backplane
P0: TE Connectivity p/n 2314578-2	**J0:** 2 TE Connectivity p/n 2309390-1

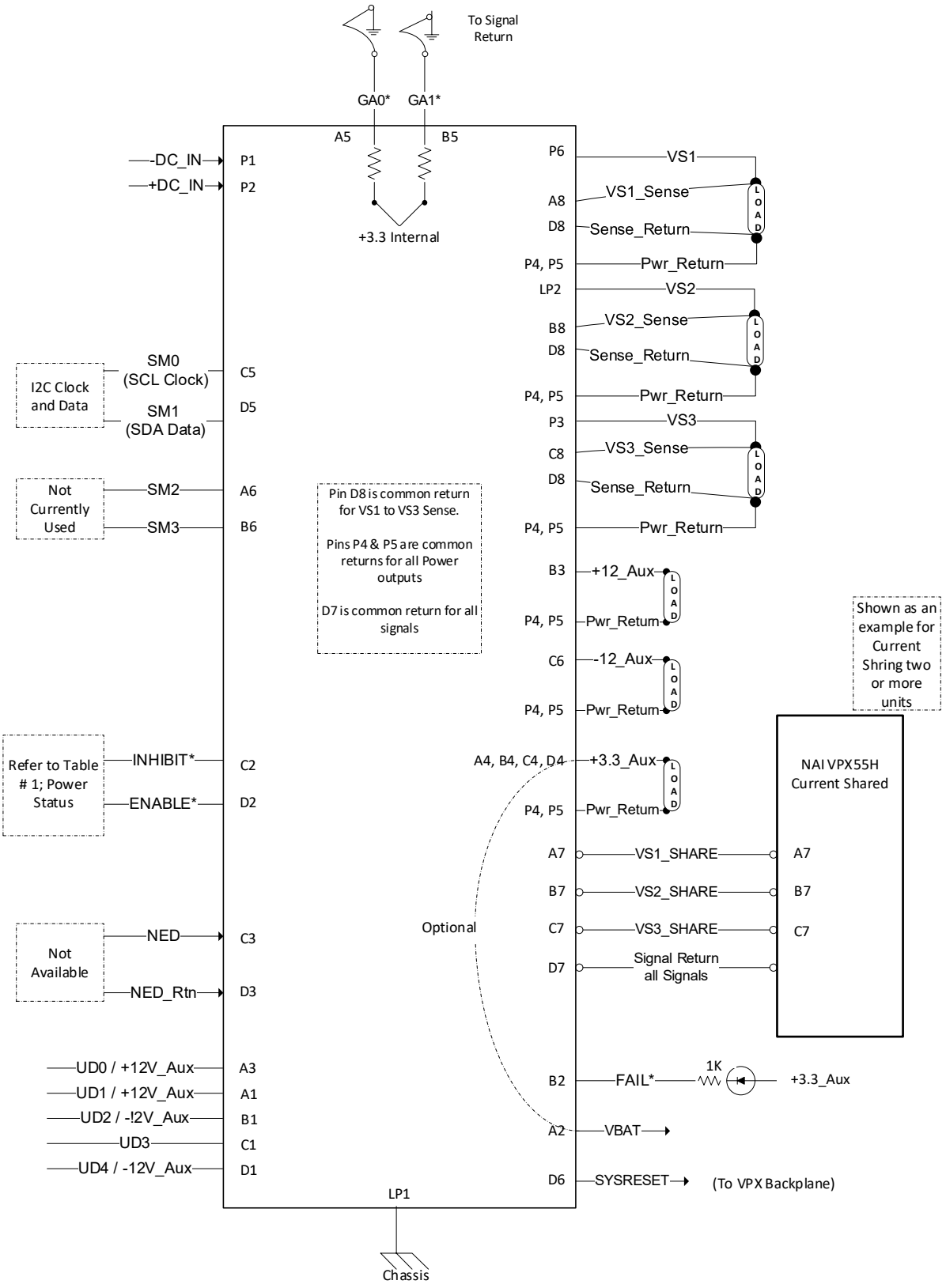
116 Wilbur Place, Bohemia, NY 11716 Tel: 631.567.1100 www.naii.com

Pinout Designations (P0)

CONNECTOR PIN OUT											
PIN #	RATED CURRENT (A)	Pin Name	Standard Configuration	12V Only SOSA™ Configuration	12V Heavy Configuration	PIN #	RATED CURRENT (A)	Pin Name	Standard Configuration	12V Only SOSA™ Configuration	12V Heavy Configuration
P1	40A	-DC_IN/ACN	-DC_IN/ACN	-DC_IN/ACN	-DC_IN/ACN	B5	<1A	GA1*	GA1*	GA1*	GA1*
P2	40A	+DC_IN/ACL	+DC_IN/ACL	+DC_IN/ACL	+DC_IN/ACL	C5	<1A	SM0	SM0	SM0	SM0
LP1	20A	CHASSIS	CHASSIS	CHASSIS	CHASSIS	D5	<1A	SM1	SM1	SM1	SM1
A1	<1A	UD1	SYNC_OUT (UD1)	SYNC_OUT (UD1)	SYNC_OUT (UD1)	A6	<1A	SM2	SM2	SM2	SM2
B1	<1A	UD2	NVMRO (UD2)	NVMRO (UD2)	NVMRO (UD2)	B6	<1A	SM3	SM3	SM3	SM3
C1	<1A	UD3	GA2* (UD3)	GA2* (UD3)	GA2* (UD3)	C6	<1.5A	-12V_AUX	-12V_AUX	Reserved	-12V_AUX
D1	<1A	UD4	3.3V_AUX_SENSE (UD4)	UD4	3.3V_AUX_SENSE (UD4)	D6	<1A	SYSRESET*	SYSRESET*	SYSRESET*	SYSRESET*
A2	<1A	VBAT	VBAT	VBAT	VBAT	A7	<1A	SHARE_1	SHARE_1	SHARE_1	SHARE_1
B2	<1A	FAIL*	FAIL*	FAIL*	FAIL*	B7	<1A	SHARE_2	SHARE_2	SHARE_2	SHARE_2
C2	<1A	INHIBIT*	INHIBIT*	INHIBIT*	INHIBIT*	C7	<1A	SHARE_3	SHARE_3	SHARE_3	SHARE_3
D2	<1A	ENABLE*	ENABLE*	ENABLE*	ENABLE*	D7	<1A	SIGNAL_RETURN	SIGNAL RETURN	SIGNAL RETURN	SIGNAL RETURN
A3	<1A	UD0	SYNC_IN (UD0)	SYNC_IN (UD0)	SYNC_IN (UD0)	A8	<1A	PO1_SENSE	SENSE, +12VDC	SENSE, +12VDC	SENSE, +12VDC
B3	<1.5A	+12V_AUX	+12V_AUX	Reserved	+12V_AUX	B8	<1A	PO2_SENSE	SENSE, +3.3VDC	SENSE, 3.3V_AUX	SENSE, +3.3VDC
C3	<1A	N/U	N/U	N/U	N/U	C8	<1A	PO3_SENSE	SENSE, +5VDC	SENSE, +12VDC	SENSE, +12VDC
D3	<1A	N/U	N/U	N/U	N/U	D8	<1A	SENSE_RETURN	SENSE RETURN	SENSE RETURN	SENSE RETURN
A4	<1.5A	3.3V_AUX	3.3V_AUX	Reserved	3.3V_AUX	P3	40A	PO3	+5VDC (Vs3)	+12VDC (Vs1)	+12VDC (Vs1)
B4	<1.5A	3.3V_AUX	3.3V_AUX	Reserved	3.3V_AUX	P4	40A	POWER_RETURN	POWER RETURN	POWER RETURN	POWER RETURN
C4	<1.5A	3.3V_AUX	3.3V_AUX	Reserved	3.3V_AUX	P5	40A	POWER_RETURN	POWER RETURN	POWER RETURN	POWER RETURN
D4	<1.5A	3.3V_AUX	3.3V_AUX	Reserved	3.3V_AUX	LP2	20A	PO2	+3.3VDC (Vs2)	3.3V_AUX	+3.3VDC (Vs2)
A5	<1A	GA0*	GA0*	GA0*	GA0*	P6	40A	PO1	+12VDC (Vs1)	+12VDC (Vs1)	+12VDC (Vs1)

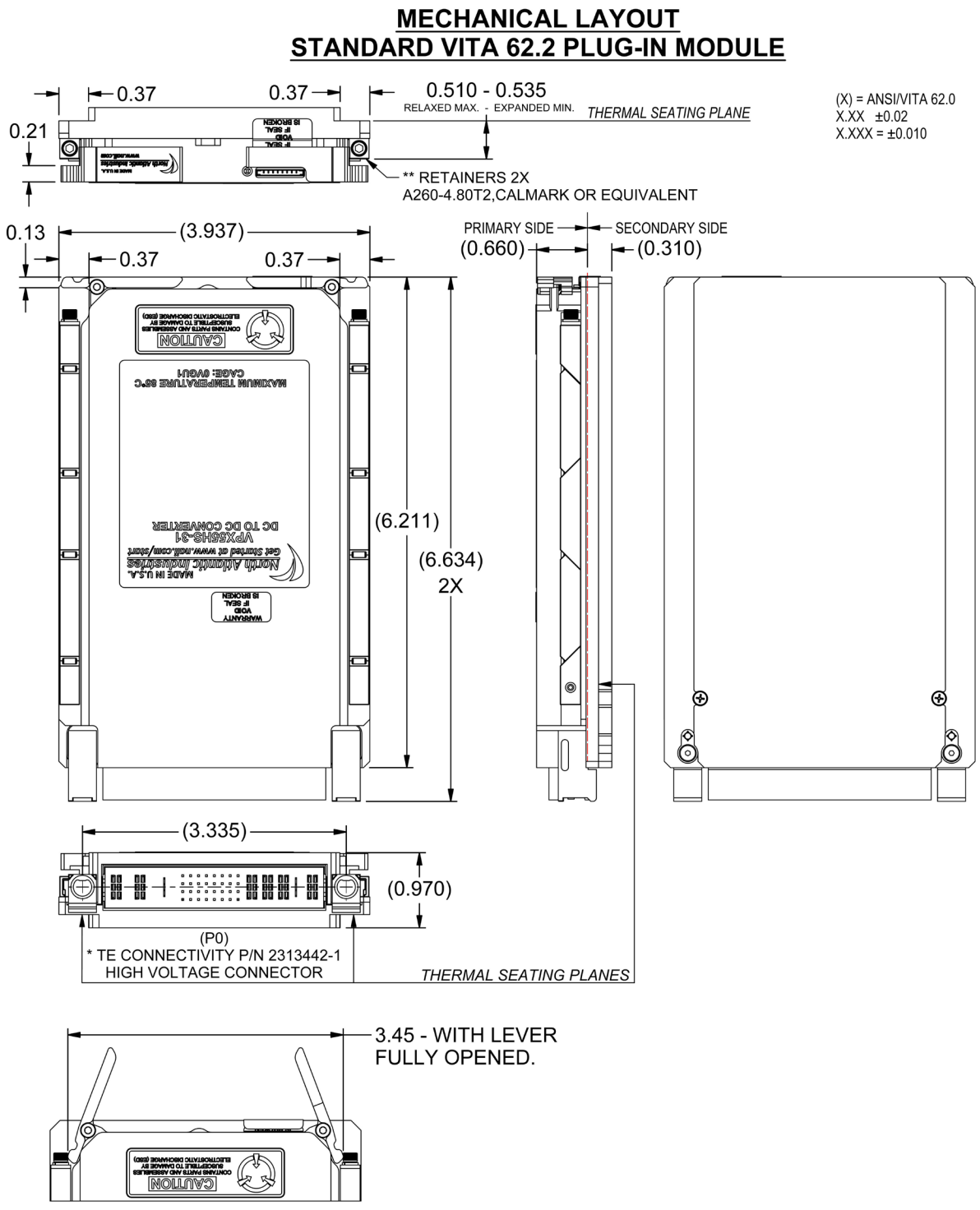
116 Wilbur Place, Bohemia, NY 11716 Tel: 631.567.1100 www.naii.com

VPX55HS-3 Connections (Shown for Standard Output Configuration)



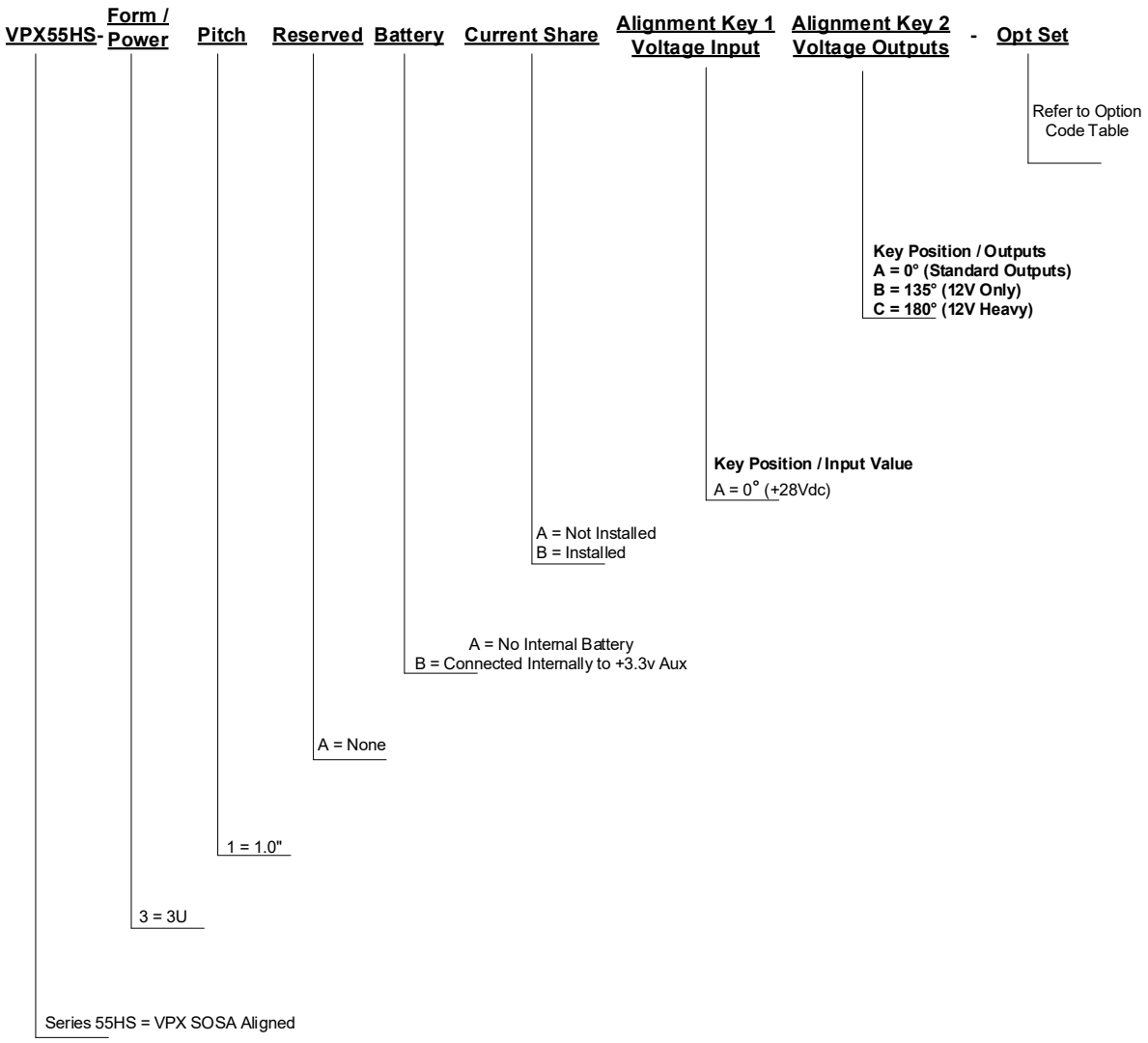
116 Wilbur Place, Bohemia, NY 11716 Tel: 631.567.1100 www.naii.com

Mechanical Layout



116 Wilbur Place, Bohemia, NY 11716 Tel: 631.567.1100 www.naii.com

Ordering Information



Example Part Number:
VPX55HS-31AABAA-00 = 3U VPX DC/DC Converter, 1.0" pitch, No Battery, Current Share on VS1 to VS3, +28Vdc Input, 750 Watts Output Power

Refer to option code table for description of option codes

Option Code Table

Code	Description
00	Standard unit, no additional options

116 Wilbur Place, Bohemia, NY 11716 Tel: 631.567.1100 www.naii.com