MIL-STD-1553 Communications, Assisted Mode Capable

FTA-FTF Function Modules

Purpose

This letter/advisory provides information and detail regarding the introduction of the improved NAI Smart Function Module(s), FTA – FTF, in comparison to the legacy FT1 – FT6 MIL-STD-1553 Module Series.

Moving forward, it is recommended that new programs requiring MIL-STD-1553 communications functions be quoted with the FTA – FTF modules, which are Assisted Mode Capable (AMC). The AMC mode advantages are detailed herein.

MIL-STD-1553 Function Description (Dual Redundant)	MOD-ID Legacy	MOD-ID AMC
1-Ch. Transformer Coupled	FT1	FTA
2-Ch, Transformer Coupled	FT2	FTB
4-Ch. Transformer Coupled	FT3	FTC
1-Ch. Direct Coupled	FT4	FTD
2-Ch, Direct Coupled	FT5	FTE
4-Ch. Direct Coupled	FT6	FTF

In addition, all “Combo” (CMx) modules that will have MIL-STD-1553 functions are expected to be “Assisted Mode Capable” (AMC). AMC capabilities are fully realized and supported in the latest NAIBrd SSKs.

Description

When new 1553 messages appear on the (FTx) 1553 module (device), the host CPU does not have access to the messages until messages “cross-over” to the host memory (Figure 1).

In the legacy FTx modules (FT1-FT6), the host CPU is responsible for accessing the device registers directly over a relatively “slow bus” or Ethernet interface to read 1553 messages into host memory one at a time. This requires multiple slow bus/interface accesses per 1553 message (Figure 2).

The improved FTA-FTF series of 1553 modules utilize the secondary (ARM) processor built into the module that is dedicated for the purpose of “assisting” the movement of 1553 messages from the 1553 device to the host interface. This is made possible through a system of FIFOs that carry command and response messages to and from the host CPU to a bare metal application running on the secondary processor (Figure 3B).

This new design also has the option of funneling all 1553 messages (per channel) to a 4k byte Message FIFO (Figure 3A) that is accessible from the host. As a result of this aided processing in conjunction with the Message FIFO, we gain the following benefits:

1. Reduced number of host CPU reads and writes to the device.
2. Reduced host memory footprint (less application memory required on the host).
3. Lower latency from 1553 bus to host memory.

To fully support DDC API compatibility in the new design, the Message FIFO does not have to be utilized and the user may instead select to use the Standard operating mode, which does not involve the Message FIFO in any way. In this (DDC mimic) mode, the response time benefits of the “assisted” design are only partially realized though it is significantly improved compared to the legacy FT module(s), especially with bulk 1553 transfers. However, the best option is to utilize the Message FIFO as it drastically shortens the latent time no matter how many messages are being read from the 1553 device. The results of our benchmarks comparing the latent times between the two assisted Modes as well as the legacy (non-assisted) FT module are presented in Figure 4. The latent time (time between host requesting 1553 messages from the device and receipt of 1553 messages in host memory) was measured as a function of the number of 1553 messages fetched from the device.

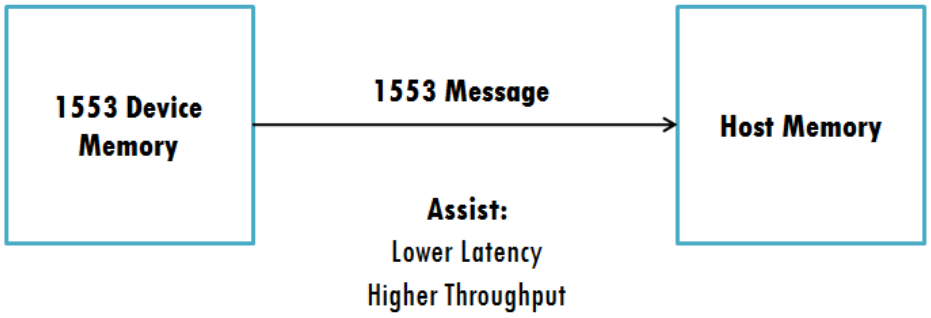

Figure 1. Host-FTx Message Transfer

Figure 1. Host-FTx Message Transfer: The goal of the new assisted design is to decrease the latent time between host request for 1553 messages and the arrival of 1553 messages into the host memory. Also, we sought to improve the throughput rate of bulk 1553 messages by utilizing a 4 Kbyte 1553 Message FIFO that interfaces to the Host.

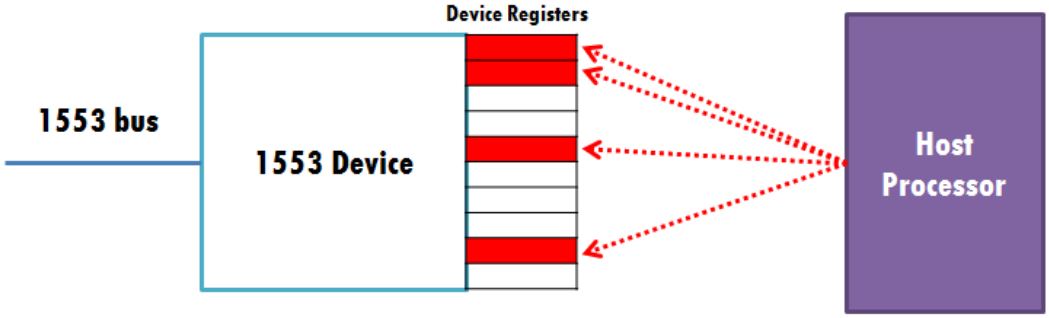

Figure 2. Message Fetch Process

Figure 2. Message Fetch Process: In the older design, 1553 messages are fetched from the 1553 device by accessing device registers directly from the host application. The dotted lines indicate relatively slow bus (or Ethernet) read/write accesses. In the old design, four slow accesses are required from the host to fetch one new 1553 message. The number of accesses increases proportionately with the number of 1553 messages to fetch from the 1553 device.

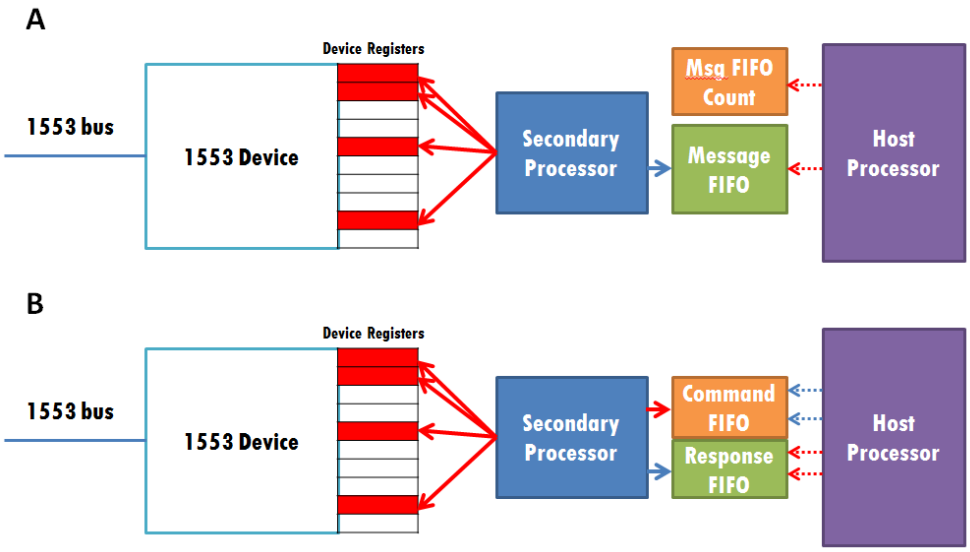

Figure 3. AMC FIFO & Bus Access Comparison

Figure 3. AMC FIFO & Bus Access Comparison: The dotted lines indicate relatively slow bus (or Ethernet) read/write accesses whereas the solid lines indicate fast bus accesses. With the new design, if the Message FIFO is utilized (A in the figure), 2 slow accesses are needed to fetch one new 1553 message. However, if the Message FIFO fills with multiple new messages before it is read, it will still only require 2 slow accesses to fetch all of the new 1553 messages that are in the Message FIFO. If the Message FIFO is not utilized in the new design (Standard mode, B in the figure), it will require 2 slow writes and at least 2 slow reads to fetch one new 1553 message. If multiple new messages are available, it will still only require 2 slow writes and 2+ slow reads to fetch all new messages. The latency between the time the 1553 data arrives on the device and reaches the host processor will be shorter using the Message FIFO mode versus the Standard mode because the Message FIFO is filled as new 1553 messages arrive whereas in the Standard mode, the write access to the Command FIFO initiates the transfer of 1553 messages from the device to the Response FIFO and when the transfer is complete (processing delay), the host can read the Response FIFO with a single slow read access. The processing delay is proportional to the number of 1553 messages transferred.

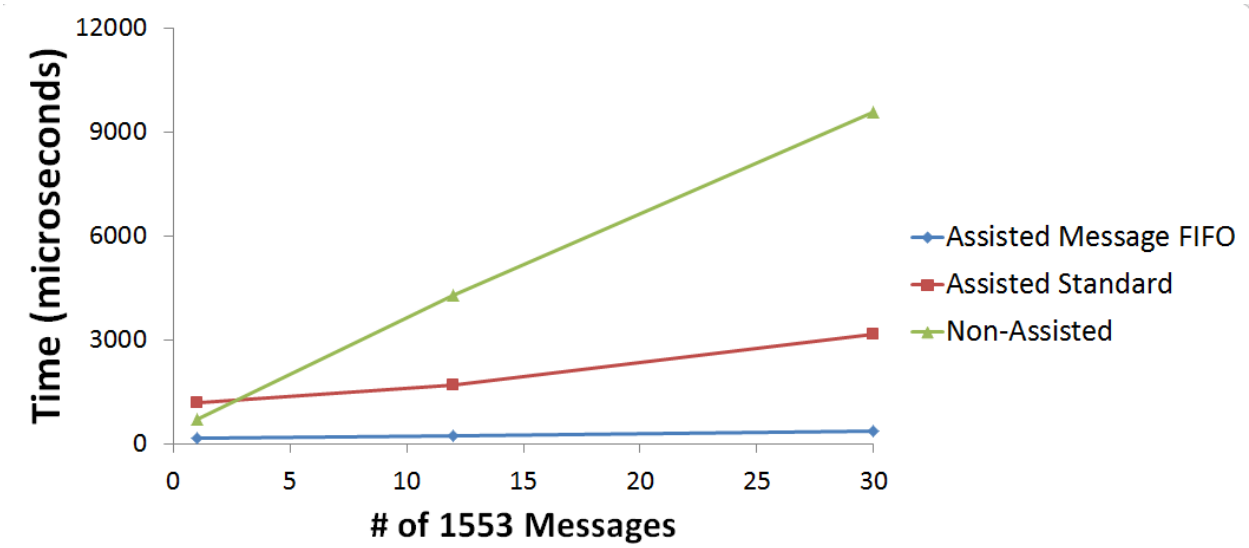

Figure 4. AMC vs. Legacy Time Transfer Comparison

Figure 4. AMC vs. Legacy Time Transfer Comparison: This graph depicts the average latent time (time required for 1553 message(s) transfer from 1553 device to host memory when initiated by the host CPU) as a function of the number of 1553 messages being transferred. The three candidates for comparison are (1) Assisted Module running in Message FIFO Mode, (2) Assisted Module running in Standard Mode and (3) the Non-Assisted (Legacy) FT Module. The average and worst-case times for these three modes are presented in Table 1.

Table 1. Average and Worst-Case Latent Times in microseconds

# 1553 Msgs	Assisted Message FIFO		Assisted Standard		Non-Assisted	
	Average	***Worst-Case***	***Average***	***Worst-Case***	***Average***	***Worst-Case***
1	163.630	182.445	1169.992	1193.958	695.578	705.235
12	239.0805	261.298	1698.532	1735.622	4286.303	5574.973
30	366.4155	399.722	3179.139	3198.554	9566.732	9610.468